REMARKS

Claims 1-5 are pending in the present application. Claims 10 and 14 have been canceled herein. Claim 2 has been amended herein for clarification. No new matter has been entered.

Claims 1-5 were rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura (US 6,653,230). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); MPEP 2131.

Claim 1 recites a method of manufacturing a memory cell comprising, *inter alia*, the steps of forming a bit line contact by forming a conductively doped polysilicon plug within a contact hole bounded by insulating side walls, and forming a doped polysilicon plug so as to define a substantially convex upper plug surface profile in contact with the bit line.

Nakamura fails to teach all elements of claim 1. For instance, Nakamura fails to teach a *substantially convex upper plug surface profile* in contact with the bit line. As shown in Figs. 3 and 4 below of the present application, the polysilicon plug 46 contacts the multilayer bit line 32 at the convex upper plug surface profile location. *See* Figs. 3 and 4

In contrast, the Nakamura figures all illustrate bit line conductive plugs 14 with rectangular shapes and flat surface profiles, not curved convex profiles as shown in Figs. 3 and 4 of the present application. Nakamura may use the word "convex" in the application; however, there is no teaching that the bit line contact plug 14 of Nakamura is convex in its upper surface profile. According to the American Heritage Dictionary, convex is defined as "[h]aving a surface or boundary that curves or bulges outward, as the exterior of a sphere".[1] None of the bit line conductive plugs 14 shown in the figures of Nakamura display a surface profile having a surface that curves or bulges upward, as in the polysilicon plug 46 of the present application. Moreover, the priority document, Japanese application 11-32177, demonstrates that the Nakamura does not consider a "convex" surface profile as part of the claimed invention, because Nakamura fails to use the word "convex" in the entirety of the Japanese Detailed Description (*see* attachment).[2]

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[1] "convex." The American Heritage® Dictionary of the English Language, Fourth Edition. Houghton Mifflin Company, 2004. Answers.com 17 May. 2006. http://www.answers.com/topic/convex

[2] Translation obtained from Patent Absract of Japan (PAJ) site: http://www19.ipdl.ncipi.go.jp/PA1/cgi-bin/PA1INIT

Nakamura appears to use "convex" narrowly to illustrate that the bit line plug 14 is an upward projection; however, Nakamura is silent as to the surface profile of the bit plugs 14. Thus, convex, as used in Nakamura, does not encompass a substantially convex *upper plug surface profile* as recited in claim 1. As a result, Nakamura does not anticipate claim 1 and its dependents thereon.

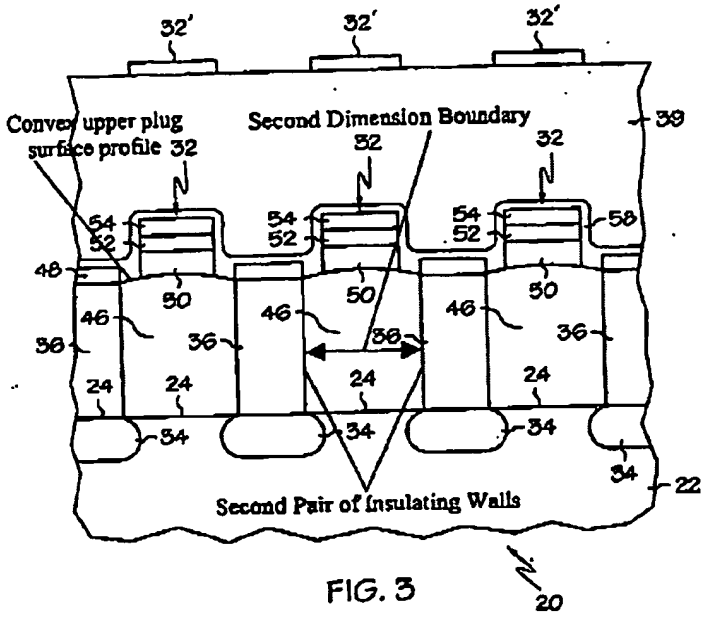


FIG. 3

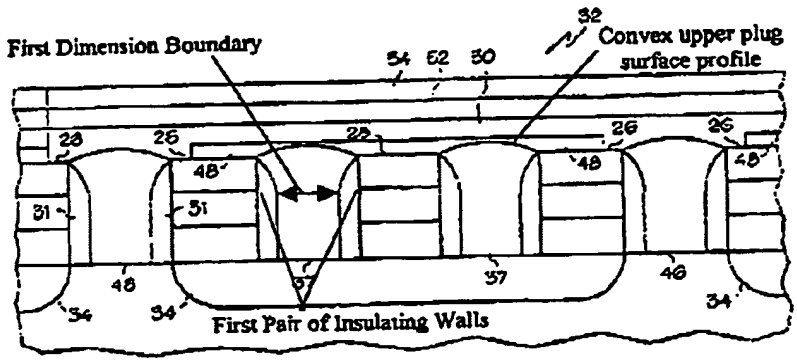
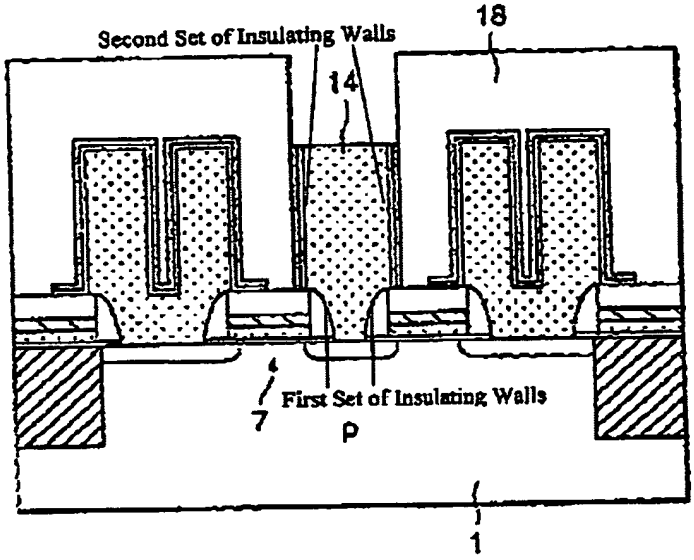


FIG. 4

Additionally, Nakamura also fails to teach the elements of dependent claim 2. Claim 2 recites a method of manufacturing a memory cell wherein the insulating side walls are formed so as to comprise a first pair of opposing insulating side walls along a first dimension and a second pair of opposing insulating side walls along a second dimension.

Referring to embodiments of present invention as shown in Figs. 3 and 4 above, the bit contact plug region 46 is bounded by the first set of insulating walls 31 (Fig. 4) along a first dimension, and is bounded along a second set of insulating wall 36 along a second dimension (Fig. 3). Fig. 3 is a cross-sectional view of the memory cell array of Fig. 2 taken along line 3-3, wherein Fig. 4 is cross-sectional view (perpendicular to the Fig. 3 view) of the memory cell array of Fig. 2 taken along line 4-4.

In contrast, Nakamura does not teach first and second pair of insulating walls along first and second dimensions respectively. The Nakamura insulating walls 15/16 and 9 bound the walls along the same dimension. *See* Fig. 6b of Nakamura below.



15 CAPACITOR INSULATING FILM
16 POLYSILICON FILM
18 SiO_2 FILM

FIG. 6B

Viewing 6b, the first and second pairs of insulating walls bound the bit line contact plug 14 along *only one dimension*, not a first and second dimension as recited in claim 2. Therefore, Nakamura also fails to anticipate claim 2.

Applicants respectfully submit that the application is in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully requested.

Respectfully submitted,

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